

AMENDMENT UNDER 37 C.F.R. § 1.111
U.S. Application No. 09/750,688
Attorney Docket No. Q62534

REMARKS

Reconsideration and allowance of this application are respectfully requested. New claims 7-10 have been added. Claims 1-10 are now pending in the application. The rejections are respectfully submitted to be obviated in view of the remarks presented herein.

Rejection Under 35 U.S.C. § 103(a) – Applicant’s Admitted Prior Art in view of Iliadis et al.

Claims 1-6 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Applicant’s admitted prior art in view of Iliadis et al. (U.S. Patent Number 5,742,606) (hereinafter “Iliadis”). The rejection is respectfully traversed.

Regarding claims 1 and 6, Applicant’s claimed invention relates to a method and apparatus of switching, such as in an input buffer type packet switching equipment. An arbiter outputs a connection permission signal to one of M input line buffers based on connection request signals outputted from the M input line buffers, and also outputs a control signal to a switch. The connection permission signal is output, at a designated slower timing interval than a normal timing interval, to an input line buffer that outputs cells to an external output line whose output line rate is slower than a corresponding input line rate.

Turning to the cited art, the background of the invention section of Applicant’s specification describes an input buffer type packet switching equipment with FIFOs (404) provided in each of the input line buffers (402), and buffers (414) provided in each output line

section (413). The buffers (414) are needed for transmission situations when an output line rate is slower than the corresponding input line rate.

Examiner maintains that the combination of Applicant's admitted prior art and Iliadis teaches each feature of the claimed invention. However, in Applicant's figure 1, the use of buffers (414) leads to undesirably large equipment size with high costs (page 2, lines 16-29). Furthermore, Applicant's figure 1 does not teach an arbiter that "outputs a connection permission signal at a designated slower timing interval than a normal timing interval to one input line buffer that outputs cells to an external output line whose output line rate is slower than a corresponding input line rate," as claimed. Examiner also readily admits in paragraph 3 of the Office Action that figure 1 fails to expressly disclose sending the connection permission signal at a designated slower timing interval than a normal timing interval to one input line buffer that outputs cells to an external output line whose output line rate is slower than a corresponding input line rate.

Iliadis does not remedy the deficiencies of Applicant's figure 1. Iliadis teaches a switch for handling packet data traffic between a plurality of input and output ports. The data traffic fall into at least two different classes with different priorities and delay sensitivities. The switch has input ports with input queues and output ports with output queues. A control means detects an overflow state in the output queues, whereupon an interrupting means inhibits transmission of at least one class of traffic for a predetermined period T. The basic idea of Iliadis is to interrupt the transmission of data with a lower priority in favor of data having a higher priority directed to the same output port (column 4, lines 5-8). When the output buffer is completely filled and

incoming packets are rejected, an overflow occurs. The interruption is then triggered and lasts for the predetermined period T. The interruption time T can be any value up to the time taken to certainly empty the output buffer. In this way, the interrupting means delays a retry of transmission of a rejected low priority data packet for time period T. The time period T delay is triggered for each input line independently by an unsuccessful attempt to transmit a low priority packet (page 4, lines 37-44).

However, there is also no teaching in Iliadis of outputting a connection permission signal at a designated slower timing interval than a normal timing interval to one input line buffer that outputs cells to an external output line whose output line rate is slower than a corresponding input line rate. Instead, Iliadis activates an interrupt of transmission of a packet. This interrupt is a delay in transmitting the packet, which lasts for a predetermined period of time T. Transmission of packets to the output buffer in Iliadis is resumed after the predetermined period T. This predetermined delay of transmission is only a delay of transmission for a predetermined period of time T, and is not a timing interval for a connection permission signal, as claimed.

Additionally, Iliadis does not prevent overflow in its output buffers. An overflow condition is detected in Iliadis, upon which transmission is inhibited for the predetermined period T. The output buffers are already full before the overflow condition is detected and transmission inhibiting is initiated. Iliadis's system enters an overflow state every time an output buffer is full. Applicant's claimed invention is distinguished in that the connection permission signal for switching cells is output to an input line buffer at a designated slower timing interval when the input line buffer outputs cells to an external output line whose output line rate is slower than a

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corresponding input line rate. In an embodiment of Applicant's invention, output buffers are even rendered unnecessary due to outputting cells to the external output line at a slower timing interval when that output line rate is slower than a corresponding input line rate. At least by virtue of the aforementioned differences, the invention defined by Applicant's claims 1 and 6 are patentable over Applicant's figure 1 in view of Iliadis. Applicant's claims 2-5 are dependent claims including all of the limitations of independent claim 1, which, as established above, distinguishes over Applicant's figure 1 in view of Iliadis. Therefore, claims 2-5 are distinguished over Applicant's figure 1 in view of Iliadis for at least the aforementioned reasons as well as for their additionally recited features. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are respectfully requested.

With further regard to claim 2, a contention controller is described which does not execute the contention control for a designated interval corresponding to the slower output line rate, when an input line buffer outputs cells to an external output line whose output line rate is slower than the corresponding input line rate. Applicant's figure 1 in view of Iliadis only delays the transmission of a packet for a predetermined period of time T. The predetermined period of time T is a given time such that an output buffer either becomes empty or is partially filled and meeting certain system criteria. This predetermined period of time T does not correspond to any output line rate. At least by virtue of this additional difference as well as the aforementioned differences, Applicant's claimed invention distinguishes over Applicant's figure 1 in view of Iliadis.

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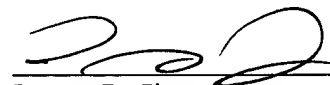
Newly Added Claims

Claims 7-10 are newly added by this Amendment and are believed to be in condition for allowance.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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